1. PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	1.8V sideband, Power Loss Notification, USB 2.0, and higher power support
DATE:	September 07, 2018
AFFECTED DOCUMENT:	PCIe M.2 Specification_Rev1.1 PCIe BGA SSD 11.5x13 ECN
SPONSOR:	Facebook, Intel, Micron, Sierra Wireless, Toshiba Memory Corp, WDC

Part I

1.1. Summary of the Functional Changes

This proposal introduces multiple features for M.2. These features include:

- Addition of 1.8V IO support type to Keys B, M, and B-M (1 pin)
- Addition of 1.8V IO Voltage source to Key M (1 pin)
- Addition of an optional pin for Power Loss Notification to Keys M, B-M, and BGA (1 pin)
- Addition of an optional pin for Power Loss Acknowledge to Keys B, M, B-M, and BGA (1 pin)
- Addition of an optional USB 2.0 interface to Key M (4 pins).
- Addition of an optional Power Disable pin for Key M (1 pin).
- Increase of static power to Key M and an addition of dynamic power including provisions to support for Keys B, M, and B-M.

The VIO 1.8 V signal is intended as an IO supply and reference voltage for host interface sideband signals PERST#, CLKREQ#, and PEWAKE# and additional signals such as SUSCLK, W_DISABLE1#, PLN#, PWRDIS, and PLA_S3#. This provides IO voltage flexibility to enable IO voltage levels other than 3.3V in the M.2 form factor. The use of the VIO 1.8 V supply is considered optional for Adapters that locally generate 1.8V from 3.3V for the host interface sideband signals.

The VIO_CFG signal is intended to provide the Platform an indication of the IO voltage capabilities of the M.2 Adapter installed. In cases where the Platform detects that an incompatible Adapter is installed, the Platform may choose to power down the VIO domain or isolate the affected sideband signals to avoid damage or interface instability.

The PLN signal is intended to trigger whatever power loss protection operation is appropriate for the PCIe function (e.g., SSD). The functionality of the power loss protection operation is expected to be developed in specifications related to the PCIe functionality (e.g., NVMe) and is not intended to interact with PCIe device or link power states. This functionality is optional.

The PLA signal is intended to signal to the Platform that the power loss protection operation has completed and that power may be safely removed.

The USB 2.0 interface is optional and intended to be used for debug or sideband communication.

The Power Disable pin is to notify the device that it shall be powered down.

The power increase support is optional as it is specific to the system implementation and power requirements of the device.

1.2. Benefits as a Result of the Changes

Host Platform and M.2 Adapter logic may benefit from a transition to lower IO voltages as silicon processes transition to smaller process nodes. Smaller M.2 form factors may benefit from the resulting power reductions of a lower IO voltage.

Some use cases for the functions implemented in M.2 and BGA form factors would benefit from an out-of-band physical signal that triggers whatever power loss protection operation is appropriate for the PCIe function (e.g., SSD).

There are increased use for HW accelerators in computing. As a result, systems are adding the connectors to support however that means a dedicated connector for one usage only. There are additional usages that can be addressed and would benefit by adding a faster debug/sideband interface and defining the peak vs. normal power of M.2 for sockets 2 and 3.

1.3. Assessment of the Impact

This change updates the pin assignments and the socket current/power requirements for M.2 socket 3.

1.4. Analysis of the Hardware Implications

This document defines usage of 3 pins for Socket 2 and 8 pins for socket 3 that previous had no or optional functionality. 4 pins are defined to support a USB 2.0 interface along with ground shields that were previously no connects. One of the ground shields overlaps DEVSLP on the system which means the host will need to decide on USB 2.0 for sideband vs. DEVSLP for SATA support. 1 pin is defined to support the host telling the device to shut off any on-Adapter power rails. 1 pin is defined for voltage configuration to configure the PCIe sidebands for 1.8V vs 3.3V which requires 3.3V tolerance for these IOs. Finally this document defines 2 pins for power loss notification which communicate that a power loss event is happening along with an Adapter response.

1.5. Analysis of the Software Implications

N/A.

1.6. Analysis of the C&I Test Implications

N/A.

1.6.1. Changes to M.2 v1.1

[Editor's note: Existing M.2 v1.1 text is black. New text is marked in blue. Material to be deleted ~~is red with strikethrough~~.]

M.2 v.1.1 Sections to be modified:

1.2. Targeted Application

The M.2 family of form factors is intended to support multiple function Adapter that include the following:

- Wi-Fi
- Bluetooth
- Global Navigation Satellite Systems (GNSS)
- Near Field Communication (NFC)
- WiGig
- WWAN (2G, 3G and 4G)
- Solid-State Storage Devices (SSD)
- Other and Future Solutions (e.g., Hybrid Digital Radio (HDR))
- Hardware Accelerator

2.4.3 System Connector Parametric Specifications

Table 13. Connector Electrical Requirements

Description	Requirement
Low Level Contact Resistance	EIA-364-23 • 55 mΩ maximum (initial) per contact • 20 mΩ maximum change allowed
Insulation Resistance	EIA-364-21 • >5 x 10~~8~~^{8} Ω @ 500 V DC
Dielectric Withstanding Voltage	EIA-364-20 • >300 V AC (RMS) @ Sea Level
Current Rating	• 0.5 A/Power Contact (continuous), 1.0A/Power contact (less than 100 us duration) • The temperature rise above ambient shall not exceed 30 °C.

Description	Requirement
	• The ambient condition is still air at 25 °C. • EIA-364-70 Method 2
Voltage Rating	50 V AC per Contact

3.2. WWAN/SSD/Other Socket 2 Adapter Interface Signals

Table 25. Socket 2 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	3.3 V (5 pins)	I	3.3 V source	3.3 V
	VIO 1.8 V	I	I/O source (low current)	1.8 V
	GND (101 pins)		Return current path.	0 V
Communication-specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the Platform chipset to reduce power and cost for the Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	3.3 V 1.8 V (Note 5)
	W_DISABLE1#	I	Active low, debounced signal when applied by the system it will disable radio operation on the Adapters that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3 V 1.8 V (Note 5)
PCIe	PERST#	I	PCIe -Reset is a functional reset to the card as defined by the *PCI Express Mini CEM Specification*.	3.3 V (note 3) 1.8 V (note 4, 5)
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini CEM Specification*. Open Drain with pull up on Platform. Active Low; also used by L1 PM Substates.	3.3 V (note 3) 1.8 V (note 4, 5)
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the Adapter supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	3.3 V (note 3) 1.8 V (note 4, 5)

Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with a pull-up on Adapter. When the Adapter supports power loss notification, this signal is used to indicate a power loss event is expected.	3.3 V 1.8 V (note 5, 6)
	PLA_S2#	O	Power Loss Acknowledge. Active low signal with weak pull-down on Platform. When the Adapter supports this function it will be driven high to indicate the Adapter has not started or completed preparations for power loss then drive low once the Adapter is done with its shutdown routing.	1.8 V (note 7)
Optional Signals	VIO_CFG	O	PCIe sideband IO voltage indication. When the Adapter supports 1.8V PCIe sideband, it must be left as high impedance.	0 V/NC

< Editor's Note these footnotes attach to Table 25>

1. LED_1# is valid for SSDs as well.
2. GPIO_9 may be defined as LED_1#, IPC_7, or SATA DAS/DSS. Host systems should use the CONFIG pins (see 3.2.12), or other mechanisms, to ensure that these signals are fully electrically compatible, or that no electrically incompatible signals are driven onto these pins of an M.2 Adapter prior to discovery of the Adapter type.
3. Key B
4. Key C
5. PCIe-based Key B and Key B-M Adapters when biased from a locally generated 1.8 V voltage on the Adapter. Must be failsafe to 3.3 V for Adapters that support 1.8V host interface sideband signaling. See Section 3.2.new.1 for more details.
6. PLN# is valid for Socket 2 Key B-M PCIe-based SSD Adapters. Socket 2 Key B WWAN devices use FULL_CARD_POWER_OFF# as a superset of PLN# functionality.
7. Socket 2 PLA_S2# functionality differs from Socket 3 and BGA PLA_S3# functionality.

3.2.11.3 General Purpose Input Output Pins

The GPIO_0 to GPIO_11 pins have configurable assignments. There are four possible functional pinouts configurations. These four configurations are called Port Config 0 to Port Config 3. In each Port Configuration, each GPIO is defined as a specific functional pin. The GPIO pin assignments are listed in Table 26.

Table 1. GPIO Pin Function Assignment per Port Configuration

	Pin	Port Config_0 (See Note 1)	Port Config_1 (See Note 2)	Port Config_2 (See Note 3)	Port Config_3 (See Note 3)	Note
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0	
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DATA2	IPC_1	
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2	
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3	
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4	
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0	
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1	
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2	
GPIO_8	28	AUDIO_3	AUDIO_3	~~RFU~~PLA_S2#	IPC_6/AUDIO_3	
GPIO_9	10	LED_1#	LED_1#	LED_1#	DAS/DSS/IPC_7	5, 6
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE	
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA	

Notes:

1. GNSS+Audio version 1
2. GNSS+Audio version 2
3. 2nd UIM/SIM Support
4. HSIC Support
5. Platform Providers may choose to implement IPC sideband instead of the LED_1# to optimize their design
6. Some host Platforms (eg., tablets) may not require support for SSD. In such configurations, Host Platform Providers may choose to implement IPC_7 on GPIO_9 instead of DAS/DSS.

< Editor's Note: add after Section 3.2.14>

3.2.new Optional Signals

3.2.new.1 VIO_CFG Signal

The VIO_CFG (IO voltage configuration) is a signal that informs the Platform that the PCIe device supports an independent IO voltage domain by physically isolating this signal. Adapters that use 3.3 V on PCIe sideband or other signals noted in Table 25 must leave VIO_CFG electrically shorted to GND. Adapters that use 1.8 V sideband signaling (either through a voltage source on the Adapter or using the VIO 1.8 V pin) must leave the VIO_CFG pin as high impedance and the affected signals on the Adapter must be tolerant to 3.3 V inputs.

Note: A 3.3 V only Adapter as indicated when VIO_CFG=GND is a hint that a 1.8 V Platform should not attempt to utilize the Adapter's signals. If an Adapter that supports 1.8 V as indicated by VIO_CFG=NC on the Adapter is in a 3.3 V Platform (i.e., 1.8 V is not supplied) then the Adapter has the option to either not function or to use the on-Adapter 1.8 V to configure itself.

3.2.new2 Power Loss Signals

The Power Loss Signals may be used to provide notification to a PCIe device that a power loss event is expected, and to provide indication that the PCIe device has successfully prepared for power loss.

3.2.new2.1 PLN# Signal

The PLN# (Power Loss Notification) is an optional signal that informs a PCIe device that a power loss event is expected. If PLN# is de-asserted before power is removed, the Adapter may return to normal operations. See 3.2.new.3 for timing information.

Any functional actions in response to this signal are not defined in this specification. Changes to the PCIe link activity due to PLN# assertion are out of scope with this specification.

3.2.new2.2 PLA_S2# Signal

The PLA_S2# (Power Loss Acknowledge) is an optional signal under Port Configuration #2 that indicates a PCIe device's preparations for a power loss are complete. When implemented, Adapters drive PLA_S2# high (de-asserted) when not in power loss processing, and until power loss processing has completed. Implementations utilizing the optional PLN# signal (see 3.2.new.1) should not require the optional PLA_S2# signal to be implemented. See 3.2.new.3 for timing information.

Any functional actions in response to this signal are not defined in this specification.

Note that as power loss preparation takes time (and continued power) some mechanism such as a timer based on out of scope mechanisms is often used to control duration of power availability when PLN# is asserted (e.g., purchasing requirements or out-of-scope reported worst-case hold up time). This time may be accelerated/minimized through the implementation of a PLA_S2# signal.

3.2.new2.3 Timing Requirements for Power Loss Signals

Figure XX shows the sequencing behavior for the power loss signals. The minimum response to recognize a time to a change in the PLN# or in the PLA_S2# signal is 1.0 µS. Any minimum assertion time or minimum negation time is out of scope for this specification.

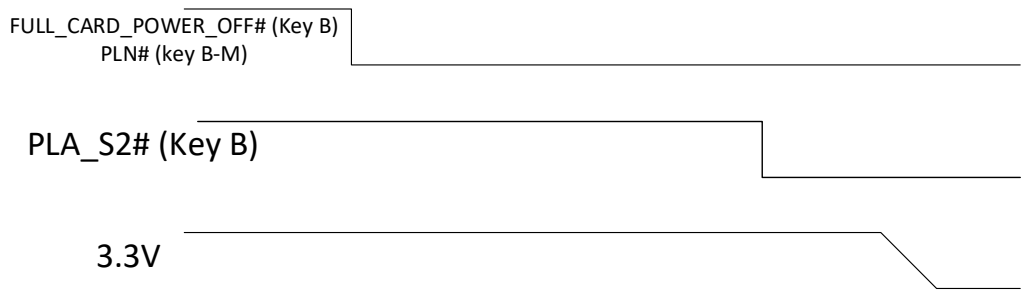

Figure xx. Power Loss Sequencing Behavior for Socket 2

Table 30. Socket 2 Key B SSIC-based WWAN Adapter Pinouts

< Editor's Note: Modified pins 8, 28, 68, and 73>

Pin	Signal	Signal	Pin
		CONFIG_2 (States 8, 9, 10, 11)	75
74	3.3 V	~~GND~~VIO_CFG	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 (States 8, 9, 10, 11)	69
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	NC	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_ PWR2/IPC_4 (I/O)(0/1.8V)	NC	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V)	NC	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_ DATA2/IPC_1 (I/O)(0/1.8V)	NC	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_ DET2/IPC_0 (I/O)(0/1.8V)	GND	39
38	NC	SSIC-RxP	37
36	UIM_PWR (O)	SSIC-RxN	35
34	UIM_DATA (I/O)	GND	33
32	UIM_CLK (O)	SSIC-TxP	31
30	UIM_RESET (O)	SSIC-TxN	29
28	PLA_S2#/GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 = NC	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	GND	11
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/1.8/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V or 3.3V)	GND	5
4	3.3 V	GND	3
2	3.3 V		

Pin	Signal	Signal	Pin
		CONFIG_3 = GND	1

Table 31. Socket 2 Key B USB3.1 Gen1-based WWAN Adapter Pinout

< Editor's Note: Modified pins 8, 28, 68, and 73>

Pin	Signal	Signal	Pin
		CONFIG_2 (States 4, 5, 6, 7)	75
74	3.3 V	~~GND~~VIO_CFG	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 (States 4, 5, 6, 7)	69
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	NC	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_ PWR2/IPC_4 (I/O)(0/1.8V)	NC	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_ CLK2/IPC_2 (I/O)(0/1.8V)	NC	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_ DATA2/IPC_1 (I/O)(0/1.8V)	NC	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_ DET2/IPC_0 (I/O)(0/1.8V)	GND	39
38	NC	USB3.0-Rx+	37
36	UIM-PWR (O)	USB3.0-Rx-	35
34	UIM-DATA (IO)	GND	33
32	UIM-CLK (O)	USB3.0-Tx+	31
30	UIM-RESET (O)	USB3.0-Tx-	29
28	PLA_S2#/GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11-WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 = GND	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND	11
8	W_DISABLE1# (I)(0/1.8/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	USB_D+	7
4	3.3 V	GND	5

Pin	Signal	Signal	Pin
2	3.3 V	GND	3
		CONFIG_3 = NC	1

Table 32. Socket 2 Key B PCIe-based WWAN Adapter Pinout

< Editor's Note: Modified pins 73, 68, 54, 52, 50, 28, 8>

Pin	Signal	Signal	Pin
		CONFIG_2 (States 2, 3, 12, 13)	75
74	3.3 V	VIO_CFG~~GND~~	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 (States 2, 3, 12, 13)	69
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8/3.3V)	GND	51
50	PERST# (I)(0/1.8/3.3V)	PERp0	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERn0	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	PETp0	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETn0	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	GND	39
38	NC	PERp1	37
36	UIM-PWR (O)	PERn1	35
34	UIM-DATA (I/O)	GND	33
32	UIM-CLK (O)	PETp1	31
30	UIM-RESET (O)	PETn1	29
28	PLA_S2#/GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 (States 2, 3, 12, 13)	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B		
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND	11
		USB_D-	9

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Pin	Signal	Signal	Pin
8	W_DISABLE1# (I)(0/1.8/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 (States 2, 3, 12, 13)	1

Table 2. Socket 2 Key B-M PCIe-based SSD Adapter Pinout

< Editor's Note: Modified pins 73, 68, 54, 52, 50, 28, and 8 >

Pin	Signal	Signal	Pin
		CONFIG_2 = GND	75
74	3.3 V	VIO_CFG~~GND~~	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 = NC	69
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	NC	67
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8/3.3V)	GND	51
50	PERST# (I)(0/1.8/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	NC	PERp1	37
36	NC	PERn1	35
34	NC	GND	33
32	NC	PETp1	31
30	NC	PETn1	29
28	PLA_S2# (O)(0/1.8V)~~NC~~	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	CONFIG_0 = GND	21
20	NC	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	LED_1#	NC	11
8	PLN# (I) (0/1.8/3.3V)~~NC~~	NC	9
6	NC	NC	7
4	3.3 V	NC	5
2	3.3 V	GND	3
		CONFIG_3 = GND	1

3.3. SSD Socket 3 Adapter Interface Signals

Table 36. Socket 3 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	3.3 V (9 pins)	I	3.3 V source	3.3 V
	VIO 1.8 V (1 pin)	I	I/O source (low current)	1.8 V (Note 1)
	GND (154 pins)		Return current path.	0 V
PCIe	PERST#	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express CEM Specification*.	3.3 V 1.8 V (Note 2)
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini CEM Specification*; Open Drain with pull up on Platform; Active Low; also used by L1 PM Substates.	3.3 V 1.8 V (Note 2)
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the Adapter supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	3.3 V 1.8 V (Note 2)
Communication-specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the Platform chipset to reduce power and cost for the Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	3.3 V 1.8 V (Note 2)
Optional Signals	VIO_CFG	O	Host PCIe sideband IO voltage indication; Must be grounded for 3.3 V only, or electrically isolated otherwise.	0 V/NC
	PWRDIS	I	Active high. Power Disable notifies the Adapter to disable the power on the Adapter.	3.3 V 1.8 V (Note 2)
USB	USB_D+, USB_D-	I/O	USB Data ± Differential serial data interface compliant to the USB 2.0 Specification.	
Power Loss Signals (Note 3)	PLN#	I	Power Loss Notification. Open drain with pull-up on Adapter. When the Adapter supports power loss notification, this signal is used to indicate a power loss event is expected.	3.3 V 1.8 V (Note 2)
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platform. When the Adapter supports this function it will be used to indicate the Adapter has completed preparations for power loss.	3.3 V 1.8 V (Note 2, 4)

< Editor's Note these footnotes attach to Table 36>

1. Required for PCIe-based Adapters that support 1.8V host interface sideband signaling.
2. Must be failsafe to 3.3 V when biased from VIO 1.8 V.
3. Power Loss Signals PLN# and PLA_S3# are valid for Socket 3 Key M PCIe-based SSD Adapters.
4. Note Socket 3 PLA_S3# functionality differs from Socket 2 PLA_S2# functionality. Socket 3 allows a host to tie together the PLA_S3# signal from multiple Adapters such that the signal remains low until all connected Adapters have completed power loss preparation (i.e., wired-or functionality)

3.3.1 Power and Grounds

PCI Express M.2 Socket 3 utilizes a single 3.3 V power source similar to that of Socket 1 and 2. The voltage source, 3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In socket 3, there is provision for nine 3.3 V pins to enable high continuous current, the same as in Socket 2 if required. The higher number of pins will help to reduce further the current resistance (IR) drop on the connector.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving GND pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

A low current consumption supply pin called VIO 1.8 V is used to supply the on-Adapter I/O buffer circuitry operating at 1.8 V. This signal is required for PCIe-based Adapters that support 1.8 V host interface sideband signaling. Platforms that make use of pinouts that include VIO 1.8 V must bring this source voltage to the relevant pin in the socket connector.

< Editor's Note 3.3.new after 3.3.4 >

3.3.new Optional Signals

3.3.new .1 VIO_CFG Signal

The VIO_CFG (IO voltage configuration) is a signal that informs the Platform that the Adapter supports an independent IO voltage domain by physically isolating this signal. Adapters that use 3.3 V on PCIe sideband or other signals noted in Table 36 must leave VIO_CFG electrically shorted to GND. Adapters that use 1.8 V sideband signaling (through using the VIO 1.8 V pin) must leave the VIO_CFG pin as high impedance and the affected signals on the Adapter must be tolerant to 3.3 V inputs.

Note: A 3.3 V only Adapter as indicated when VIO_CFG=GND is a hint that a 1.8 V Platform should not attempt to utilize the Adapter's signals. If an Adapter that supports 1.8 V as indicated by VIO_CFG=NC on the Adapter is in a 3.3 V Platform (i.e., 1.8 V is not supplied) then the Adapter has the option to either not function or to sense VIO 1.8 V to configure itself.

3.3.new.2 PWRDIS

The Power Disable (PWRDIS) signal is an optional signal used to disable the power on the M.2 Adapter. When this signal is asserted, the Adapter shall disable the power to the circuits on the Adapter. The PCIe link may not be functional during this time. The host may provide power when PWRDIS is asserted. When this signal is de-asserted the Adapter shall allow power to the circuits on the Adapter.

This signal meets 1.8V signaling as defined in Table 41. The Power Disable (PWRDIS) AC characteristics are provided in Table xx

Table xx. PWRDIS AC characteristics

Parameter	Min	Max	Unit
PWRDIS asserted hold time		5	s
PWRDIS de-asserted hold time		0.1	s
Note: The hold time is the length of time PWRDIS is asserted or negated. This timing shall include time of 1 us to recognize a change on PWRDIS (de-bounce time).			

3.3.new2. USB Interface

See section 3.1.5, USB Interface for a detailed description of the USB signals.

3.3.new3. Power Loss Signals

The Power Loss Signals are an optional signal pair that inform a PCIe device that a power loss event is expected, and that indicates a PCIe device's preparations for a power loss are complete.

3.3.new3.1 PLN# Signal

See section 3.2.new2.1, PLN# Signal for a more detailed description of PLN# and 3.3.new3.3 for timing information.

3.3.new3.2 PLA_S3# Signal

The Power Loss Acknowledge signal is an optional signal to be used to indicate the Adapter has completed preparations for power loss. The open-drive requirement on the Adapter allows a host to tie together the PLA_S3# signal from multiple Adapters such that the signal remains low until all connected Adapters have completed power loss preparation (i.e., wired-or functionality).

Any functional actions in response to this signal are not defined in this specification.

Note that as power loss preparation takes time (and continued power) some mechanism such as a timer based on out of scope mechanisms is often used to control duration of power availability when PLN# is asserted (e.g., purchasing requirements or out-of-scope reported worst-case hold up time). This time may be accelerated/minimized through the implementation of a PLA_S3# signal.

3.3.new3.3 Timing Requirements for Power Loss Signals

Figure XX shows the sequencing behavior for the power loss signals. The minimum response to recognize a time to a change in the PLN# or in the PLA_S3# signal is 1.0 µS. Any minimum assertion time or minimum negation time is out of scope for this specification.

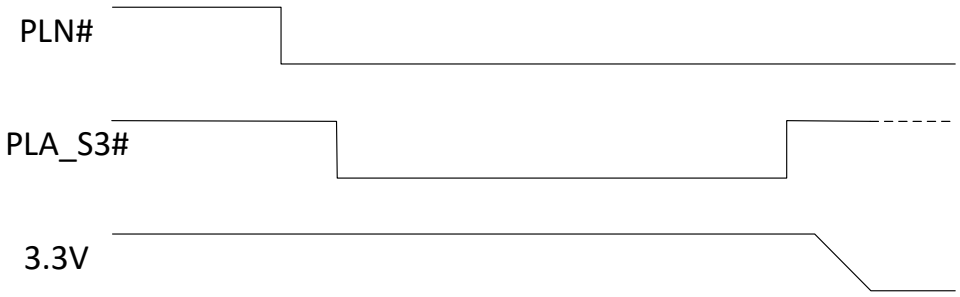


Figure xx. Power Loss Sequencing Behavior for Socket 3

3.3.5. Socket 3 Connector Pinout Definitions

All pinouts tables in this section are written from the Adapter point of view when referencing signal directions.

Table 37 and Table 38 list the signal pinouts for the Add-in Card edge card connector. Table 37 lists the SATA based solution pinouts. Table 38 lists the PCIe Multi-lane based solution pinouts.

Table 38. Socket 3 PCIe-based Adapter Pinouts (Key M)

< Editor's Note: changed pins 73, 54, 52, 50, 38, 36, 34, 32, 30, 22, 8, and 6>

Pin	Signal	Signal	Pin
		GND	75
74	3.3V	VIO_CFG~~GND~~	73
72	3.3V	GND	71
70	3.3V	PEDET (NC-PCIe)	69
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	NC	67
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8/3.3V)	GND	51
50	PERST# (I)(0/1.8/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	GND~~NC~~	PERp1	37
36	USB_D-~~NC~~	PERn1	35
34	USB_D+~~NC~~	GND	33
32	GND~~NC~~	PETp1	31
30	PLA_S3# (O)(0/1.8/3.3V)~~NC~~	PETn1	29
28	NC	GND	27
26	NC	PERp2	25
24	NC	PERn2	23
22	VIO 1.8 V~~NC~~	GND	21
20	NC	PETp2	19
18	3.3V	PETn2	17
16	3.3V	GND	15
14	3.3V	PERp3	13
12	3.3V	PERn3	11
10	LED_1# (O)	GND	9
8	PLN# (I) (0/1.8/3.3V)~~NC~~	PETp3	7
6	PWRDIS (I) (0/1.8/3.3V)~~NC~~	PETn3	5
4	3.3V	GND	3
2	3.3V	GND	1

< Editor's Note 4.3.new after 4.3.4, Table value is defined in incorporation into spec>

3.4. BGA SSD Interface Signals

Table 39. BGA SSD System Interface Signal Table

< Editor's Note: At end of table>

Interface	Signal Name	I/O	Function	Voltage
Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with pull-up on Platform. When the Module supports power loss notification, this signal is used to indicate a power loss event is expected.	1.8 V
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platform. When the Module supports this function it will be used to indicate the Module has completed preparations for power loss.	1.8 V

< Editor's Note: After 3.4.5.7>

3.4.new Power Loss Signals

The Power Loss Signals are an optional signal pair that inform a PCIe device that a power loss event is expected, and that indicates a PCIe device's preparations for a power loss are complete.

3.4.new.1 PLN# Signal

See section 3.2.new2.1, PLN# Signal for a more detailed description of PLN# and 3.3.new3.3 for timing information.

3.4.new.2 PLA_S3# Signal

See section 3.3.new3.2, PLA_S3# signal for a more detailed description of PLA_S3#.

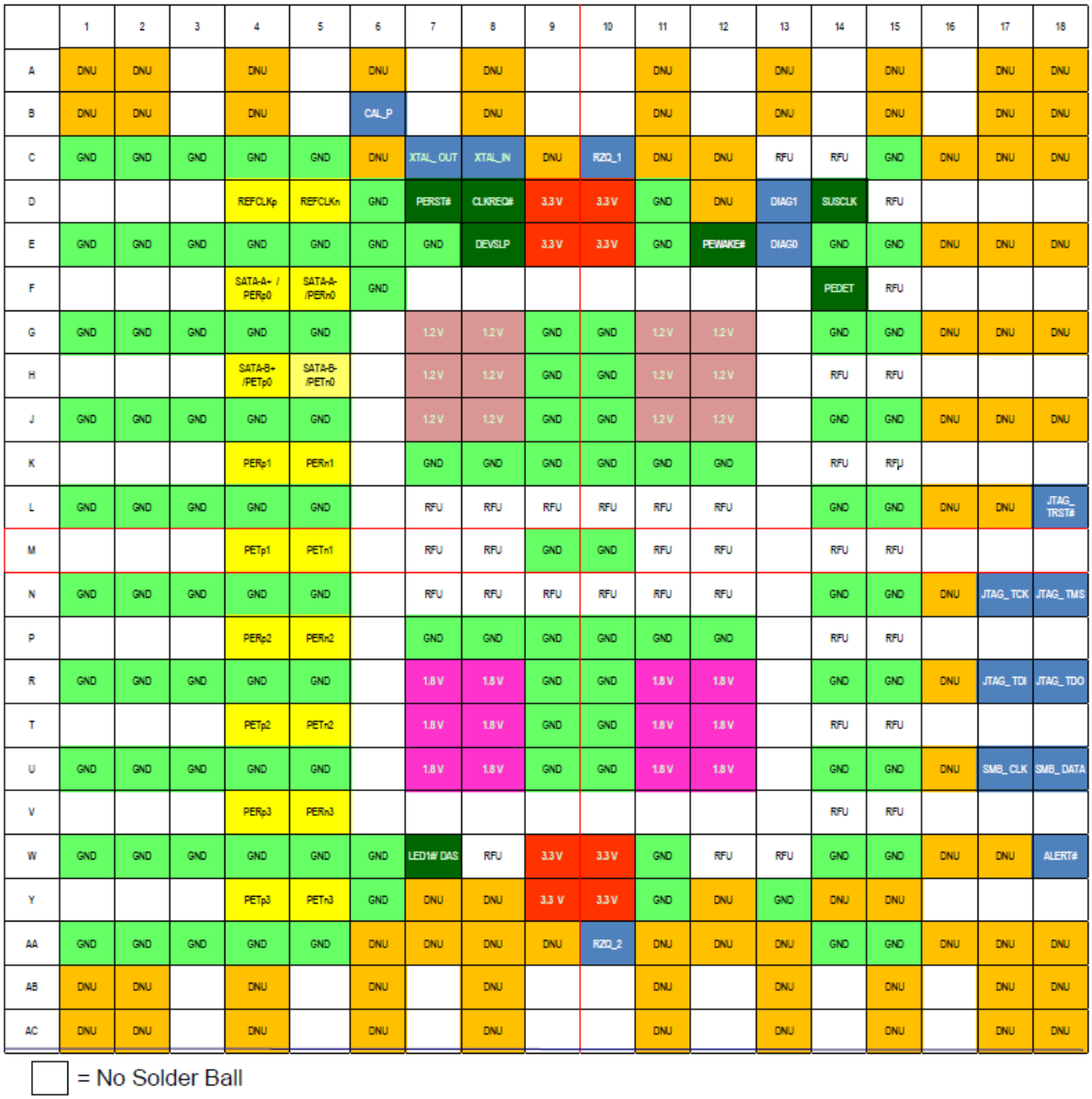
3.4.new.3 Timing Requirements for Power Loss Signals

See section 3.3.new3.3, Timing Requirements for Power Loss Signals.

<Editor's Note: In Figure 104 replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3 V	3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PETp2	PETn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	3.3 V	3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

= No Solder Ball

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

<Editor's Note: In Figure 105 replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>

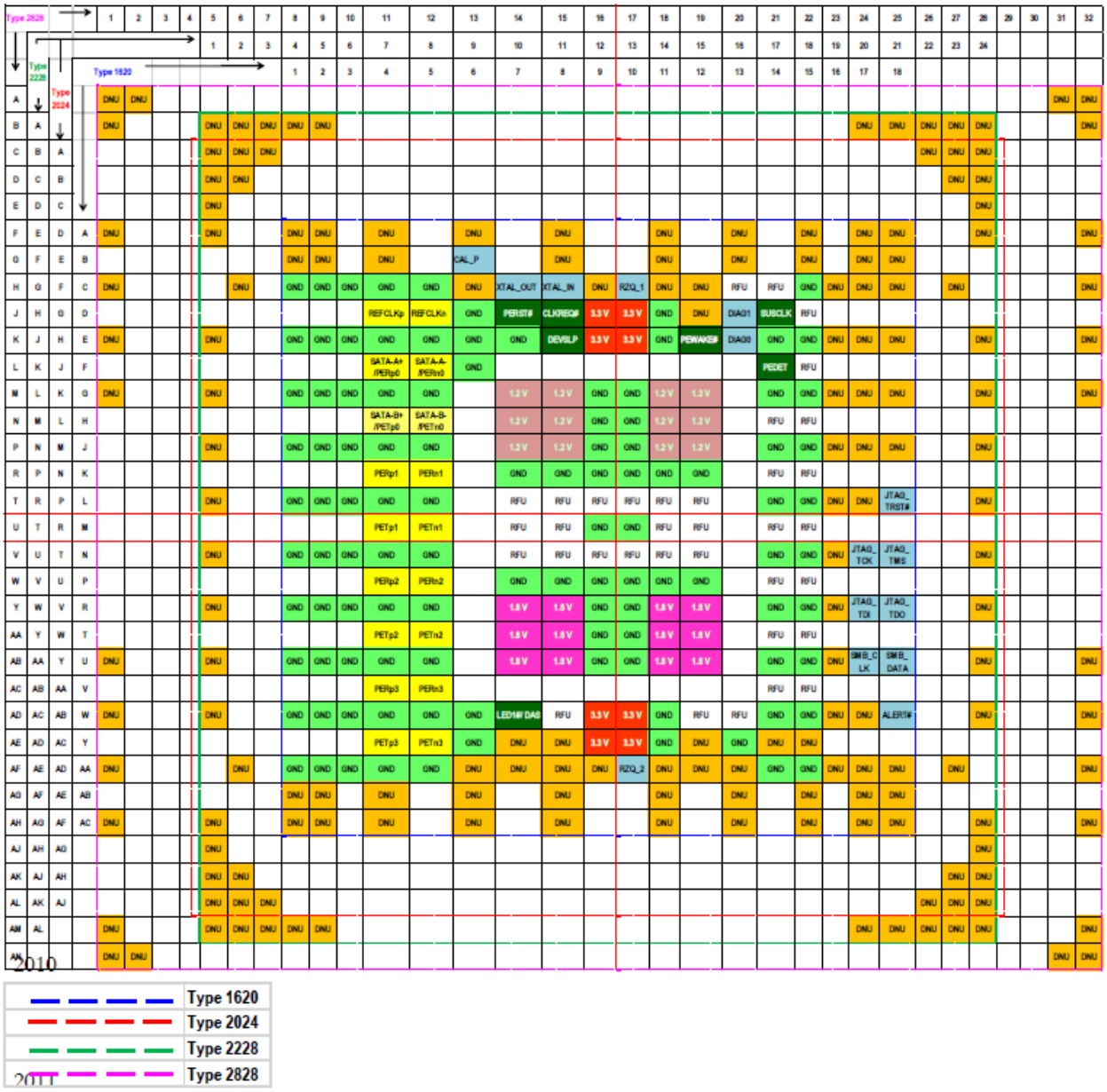


Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)

4.2. 1.8 V Logic Signal Requirements

The 1.8 V card logic levels for single-ended digital signals (PCIe sideband, SDIO, UART, I2C, PCM/I2S, SMBus, PWRDIS, PLN#, PLA_S2#, PLA_S3#, etc.) are given in Table 41. This table also defines the signaling levels for BGA SSD defined single-ended signals such as (PERST#, CLKREQ#, PEWAKE#, SUSCLK, SMB_CLK, SMB_DAT, ALERT#, PLN#, PLA#).

<Editor's Note: New section added after 4.2>

4.new. Electrical Requirements for M.2 Adapters

4.new.1. Voltage Supply Power-on Sequencing

The host should apply the following sequencing recommendations for Platforms that implement the VIO 1.8 V supply. During power-on:

- After the voltage on the 3.3 V supply or the voltage on the VIO 1.8 V supply reach 300mV, the voltage on +3.3V should remain greater than VIO 1.8 V by at least 200mV.

If the power-on sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

4.new.2. Voltage Supply Power-off Sequencing

The host should apply the following sequencing recommendations for Platforms that implement the VIO 1.8 V supply. During power-off:

- Before the voltage on the 3.3 V supply and the voltage on the VIO 1.8 V supply reach 300 mV, the voltage on the 3.3 V supply should remain greater than voltage on the VIO 1.8 V supply by 200 mV.
- After both the voltage on the 3.3 V supply and the voltage on the VIO 1.8 V supply are below 300 mV, there is no specified relationship between them.
- The voltage on all supplies should remain below 100 mV for at least 1 ms before the power-on sequence is restarted.

If the power-off sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

<Editor's Note: Sections 4.3 and 4.4 renumbered based on above section insertion>

4.4. Power

The M.2 Adapter utilizes a single regulated power rail of 3.3 V provided by the Platform. In some pinout Adapter, there is a dedicated VIO supply pin called VIO 1.8 V that is intended to only bias the I/O circuitry of the Adapter. Signals that are powered by VIO 1.8 V in Key M PCIe-based Adapters or by an internal voltage source for Key B and Key B-M specifically must be 3.3V tolerant in the event that VIO 1.8 V is not provided by the Platform. The main 3.3 V and the VIO voltage rail sources on the Platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs require host (driver) intervention after a power-on.

The number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pinout.

- Type 1630, intended for Socket 1, has two power pins allocated in the pinouts that supports up to 1 A continuous.
- Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and support up to 2 A continuous.
- The Socket 2 board types have five power pins in their pinouts and support up to 2.5 A continuous. To ensure current balancing between power pins, the resistance between any 3.3V pin across the connector shall be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.
- The Socket 3 board types, with a single Add-in Card Key, have nine power pins but support up to ~~2.5~~3.5 A continuous. Current above continuous 2.5A requires sufficient power dissipation capability (e.g. airflow, heat sink, etc.). This capability is outside the scope of this specification. To ensure current balancing between power pins, the resistance between any 3.3V pin across the connector shall be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.
- The ~~four~~ extra power pins beyond the amount of pins that support the continuous current enable reduced IR drop for these devices.

Table 46. Power Rating Table for M.2 Modules with Connectors

Key	Power Rail	Voltage Tolerance	Current Consumption Limit	
			Peak[1] mA Max Avg @ 100 µs	**Normal[2] mA** Max Avg @ 1 s
A	3.3 V	± 5%	2000	
~~B~~	~~3.3 V~~	~~± 5%~~	~~2500~~	
B	3.3 V	± 5%	5000[5,6]	2500[5]
B	V_{BAT}	3.135 V – 4.4 V	2500	
C	3.3 V	± 5%	2500	
C	V_{BAT}	3.135 V – 4.4 V	2500	
C	1.8 V[3]	± 5.55%[4]	70	
D	RFU	RFU	RFU	RFU
E	3.3 V	± 5%	2000	
F	RFU	RFU	RFU	RFU
G	N/A	N/A	N/A	N/A
H	RFU	RFU	RFU	RFU
J	RFU	RFU	RFU	RFU
K	RFU	RFU	RFU	RFU
L	RFU	RFU	RFU	RFU
~~M~~	~~3.3 V~~	~~± 5%~~	~~2500~~	
M	3.3 V	± 5%	7000[5,6]	3500[5]
M	1.8 V[3]	± 5.55%[4]	70	

[1] Peak is ~~T~~the maximum highest averaged current value over any 100 µs period

[2] Normal is ~~T~~the The maximum highest averaged current value over any 1 s period

[3] Pin name VIO 1.8 V

[4] 1.7 V to 1.9 V Range

[5] Normal currents above 2500 mA assume sufficient power dissipation capability by the Platform. This capability is outside the scope of this specification. The maximum power of device may be controlled through function specific capabilities (e.g., for SSDs see NVMe).

[6] The peak current's duty cycle shall ensure that the normal current is not violated.

5.2.1.2. **Socket 2 Pinout (Mechanical Key B) On Platform**

Table 52. Socket 2 Pinouts Diagram (Mechanical Key B) On Platform

< Editor's Note: changed pins 8, 28, 50, 52, 54, 68, and 73>

Pin	Signal	Signal	Pin
		CONFIG_2	75
74	3.3 V	VIO_CFG (I) or GND	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1	69
68	SUSCLK(32kHz) (O)(0/1.8/3.3V)	RESET# (O)(0/1.8V)	67
66	SIM DETECT (O)	ANTCTL3 (I)(0/1.8V)	65
64	COEX_RXD (I)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
62	COEX_TXD (O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (I)(0/1.8V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8V/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8V/3.3V)	GND	51
50	PERST# (O)(0/1.8V/3.3V)	PETp0/SATA-A+	49
48	GPIO_4 (I/O)(0/1.8V)	PETn0/SATA-A-	47
46	GPIO_3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 (I/O)/ALERT# (I)/(0/1.8V)	PERp0/SATA-B-	43
42	GPIO_1 (I/O)/SMB_DATA (I/O)/(0/1.8V)	PERn0/SATA-B+	41
40	GPIO_0 (I/O)/SMB_CLK (I/O)/(0/1.8V)	GND	39
38	DEVSLP (O)	PETp1/USB3.0-Tx+/SSIC-TxP	37
36	UIM-PWR (I)	PETn1/USB3.0-Tx-/SSIC-TxN	35
34	UIM-DATA (I/O)	GND	33
32	UIM-CLK (I)	PERp1/USB3.0-Rx+/SSIC-RxP	31
30	UIM-RESET (I)	PERn1/USB3.0-Rx-/SSIC-RxN	29
28	PLA_S2# (I)/GPIO_8 (I/O) (0/1.8V)	GND	27
26	GPIO_10 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
24	GPIO_7 (I/O) (0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
22	GPIO_6 (I/O)(0/1.8V)	CONFIG_0	21
20	GPIO_5 (I/O)(0/1.8V)	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
10	GPIO_9/DAS/DSS# (I/O)/LED_1# (I)(0/3.3V)	GND	11
8	W_DISABLE1# (O)(0/1.8/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (O) (0/1.8V or 3.3V)	USB_D+	7
4	3.3 V	GND	5

Pin	Signal	Signal	Pin
2	3.3 V	GND	3
		CONFIG_3	1

5.3. SSD Socket; Socket 3 (Mechanical Key M)

< Editor's Note: changed pins 6, 8, 22, 30, 32, 34, 36, 38, 50, 52, 54, 68, and 73>

Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	VIO_CFG (I) or GND	73
72	3.3 V	GND	71
70	3.3 V	PEDET (NC-PCIe/GND-SATA)	69
68	SUSCLK(32kHz) (O)(0/1.8/3.3V)	NC	67
	CONNECTOR KEY M	CONNECTOR KEY M	
	CONNECTOR KEY M	CONNECTOR KEY M	
	CONNECTOR KEY M	CONNECTOR KEY M	
	CONNECTOR KEY M	CONNECTOR KEY M	
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8V/3.3V) or NC	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8V/3.3V) or NC	GND	51
50	PERST# (O)(0/1.8V/3.3V) or NC	PETp0/SATA-A+	49
48	NC	PETn0/SATA-A-	47
46	NC	GND	45
44	ALERT# (I) (0/1.8V)	PERp0/SATA-B-	43
42	SMB_DATA (I/O) (0/1.8V)	PERn0/SATA-B+	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	DEVSLP (SATA) or GND (PCIe) (O)	PETp1	37
36	USB_D- or NC	PETn1	35
34	USB_D+ or NC	GND	33
32	GND or NC	PERp1	31
30	PLA_S3# (O)(0/3.3V) or NC	PERn1	29
28	NC	GND	27
26	NC	PETp2	25
24	NC	PETn2	23
22	VIO 1.8 V or NC	GND	21
20	NC	PERp2	19
18	3.3 V	PERn2	17
16	3.3 V	GND	15
14	3.3 V	PETp3	13

Pin	Signal	Signal	Pin
12	3.3 V	PETn3	11
10	DAS/DSS# (I/O)/LED_1# (I)(0/3.3V)	GND	9
8	PLN# (I) (0/1.8V/3.3V) or NC	PERp3	7
6	PWRDIS (O)(0/1.8V/3.3V) or NC	PERn3	5
4	3.3 V	GND	3
2	3.3 V	GND	1

Although the pinouts in Table 54 allocates four additional 3.3 V power pins, it is not intended to increase the current sinking capability of the Adapter without sufficient power dissipation capability from the Platform. This capability is outside the scope of this specification. The intention is to further reduce the IR drop of the power under extreme high current cases and increase the robustness of the SSD devices. For higher power applications, the resistance between any two 3.3 V pins on the host and device shall be less than 15 mΩ. The maximum power consumption of this socket remains as identified in section 3.3, SSD Socket 3 System Interface Signals. This Socket will also accept SSD devices Add-in Cards that employ a Dual Module key on Module scheme. The SMBus interface available on Socket 3 may be~~is~~ used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.

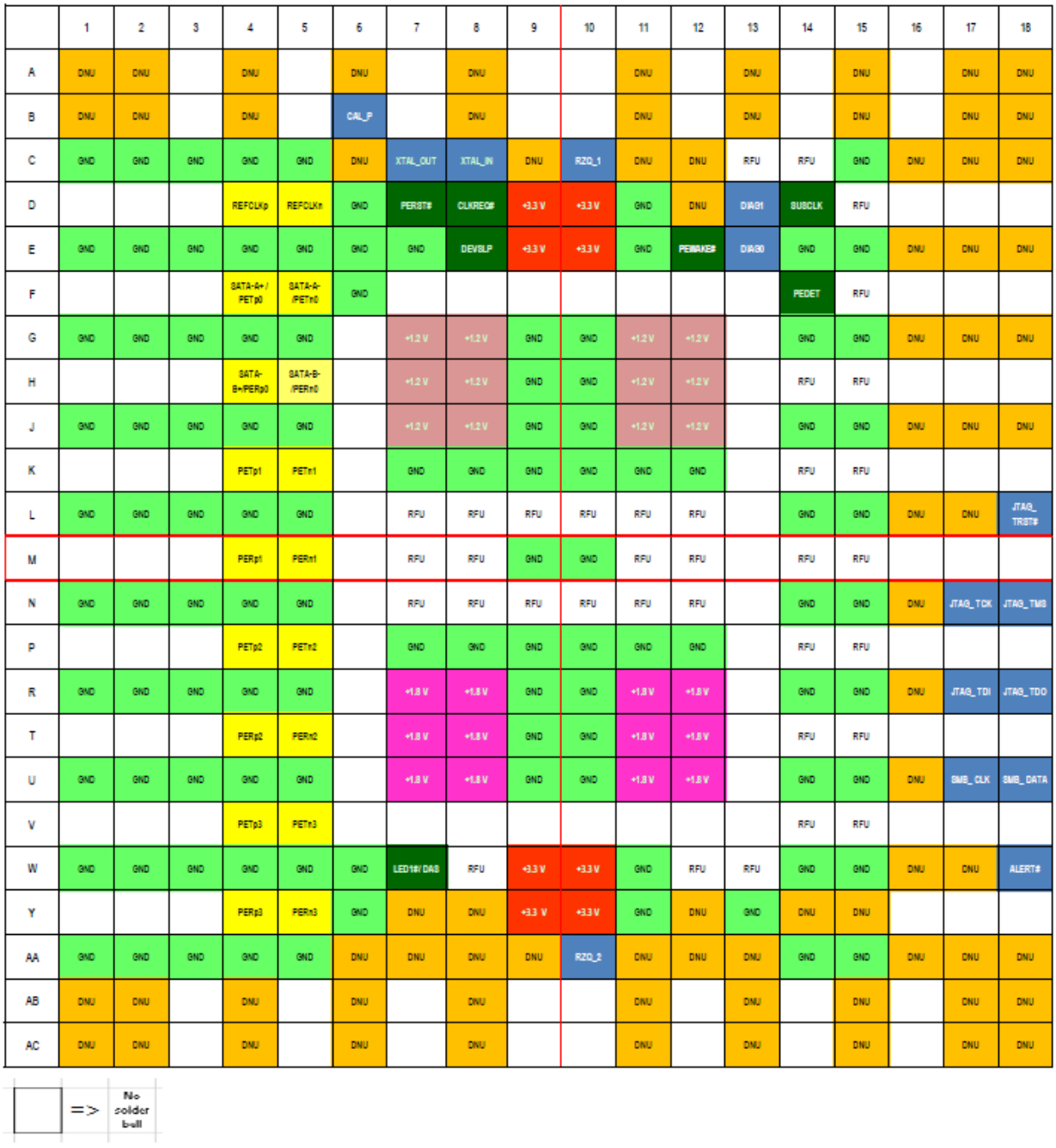
Grounds at pin 30 and pin 38 are used with Platform support of USB 2.0 only.

5.4. Soldered Down Pinouts Definitions

<Editor's Note: In Figure 111, replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	+3.3 V	+3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- /PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B- /PERn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PERp2	PERn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAB	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	+3.3 V	+3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

=> No solder ball

Figure 111. Type 1620 BGA Pinout On Platform (Top View)

<Editor's Note: In Figure 112, replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>

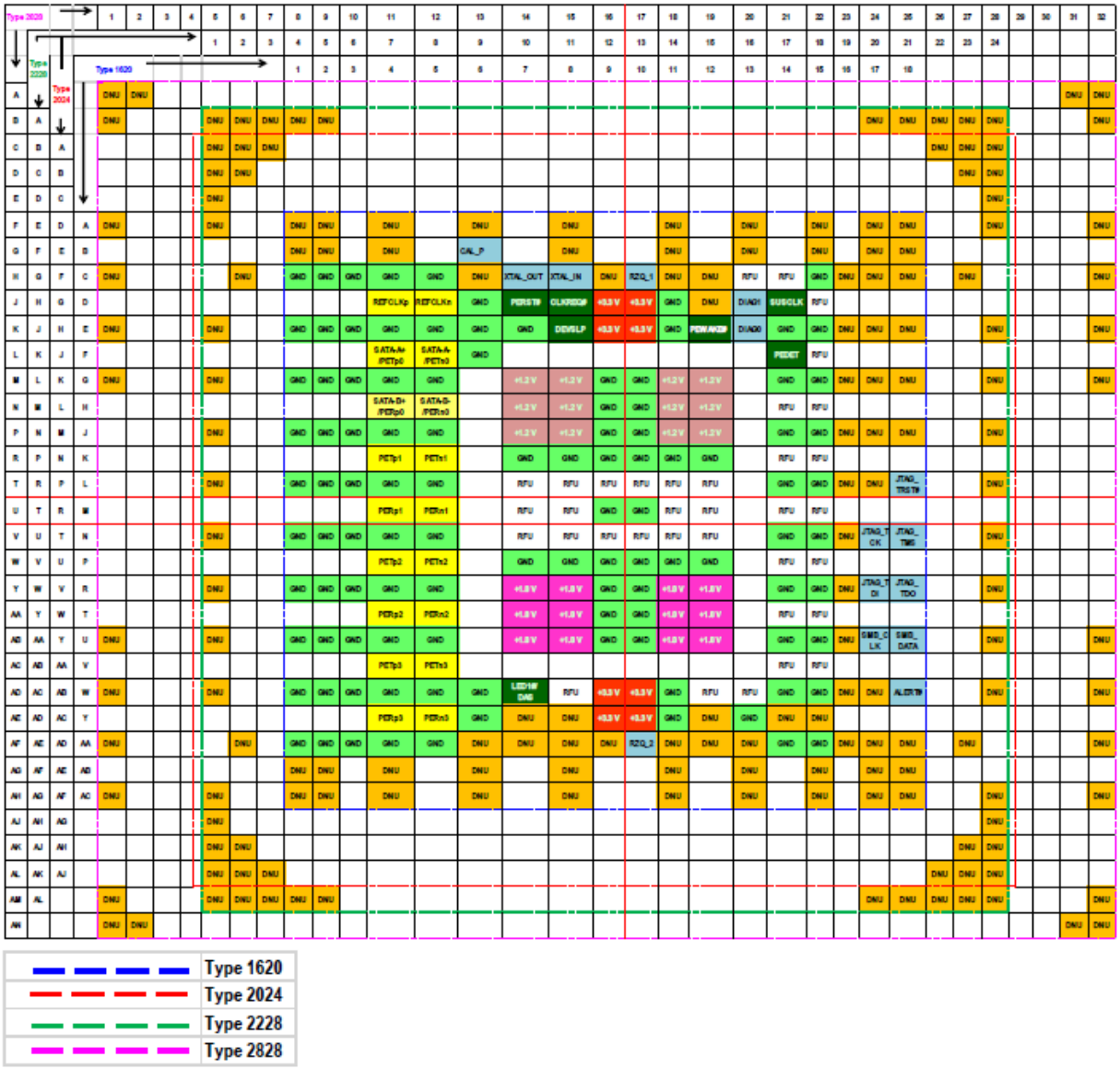


Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA Pinout On Platform (Top View)

1.6.2. Changes to PCIe BGA SSD 11.5x13 ECN.

[Editor's note: Existing PCIe BGA SSD 11.5x13 ECN text is black. New text is marked in blue. Material to be deleted ~~is red with strikethrough~~.]

3.4 BGA SSD Interface Signals

<Table and <Ed. Note: R12g is confused here – table labels belong before the table>

Table 39. BGA SSD System Interface Signal Table for Types 1620, 2024, 2228, and 2828

Interface	Signal Name	I/O	Function	Voltage
Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with pull-up on Platform. When the Module supports power loss notification, this signal is used to indicate a power loss event is expected.	PWR_2
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platform. When the Module supports this function it will be used to indicate the Module has completed preparations for power loss.	PWR_2

Table 39a. BGA SSD System Interface Signal Table for Type 1113

Interface	Signal Name	I/O	Function	Voltage
Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with pull-up on Platform. When the Module supports power loss notification, this signal is used to indicate a power loss event is expected.	PWR_2
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platform. When the Module supports this function it will be used to indicate the Module has completed preparations for power loss.	PWR_2

<Ed. Note 3.4.new is the same as in the ECR for M.2 1.1>

3. 4.new Power Loss Signals

The Power Loss Signals are an optional signal pair that inform a PCIe device that a power loss event is expected, and that indicates a PCIe device's preparations for a power loss are complete.

3.4.new.1 PLN# Signal

See section 3.2.new2.1, PLN# Signal for a more detailed description of PLN# and 3.3.new3.3 for timing information.

3.4.new.2 PLA_S3# Signal

See section 3.3.new3.2, PLA_S3# for a more detailed description of PLA_S3#.

3.4.6. BGA SSD Soldered-Down Module Pin-out

<Editor's Note: Identical to M2. 1.1 changes

In Figure 104 replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>

REQUEST REQUEST REQUEST REQUEST REQUEST REQUEST

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_ OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PETp2	PETn2		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1#/ DAS	RFU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

<Editor's Note: In Figure 105 replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>

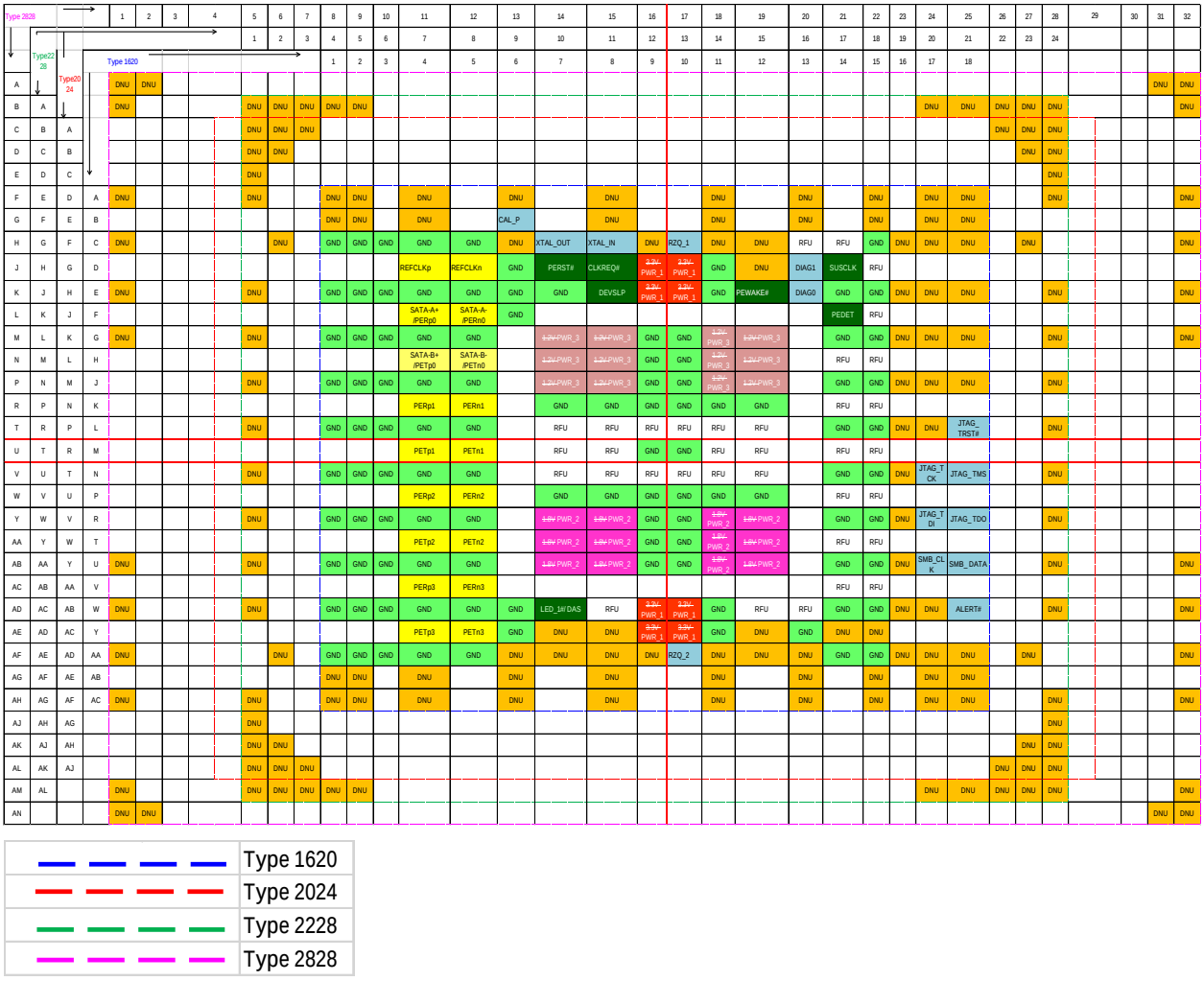
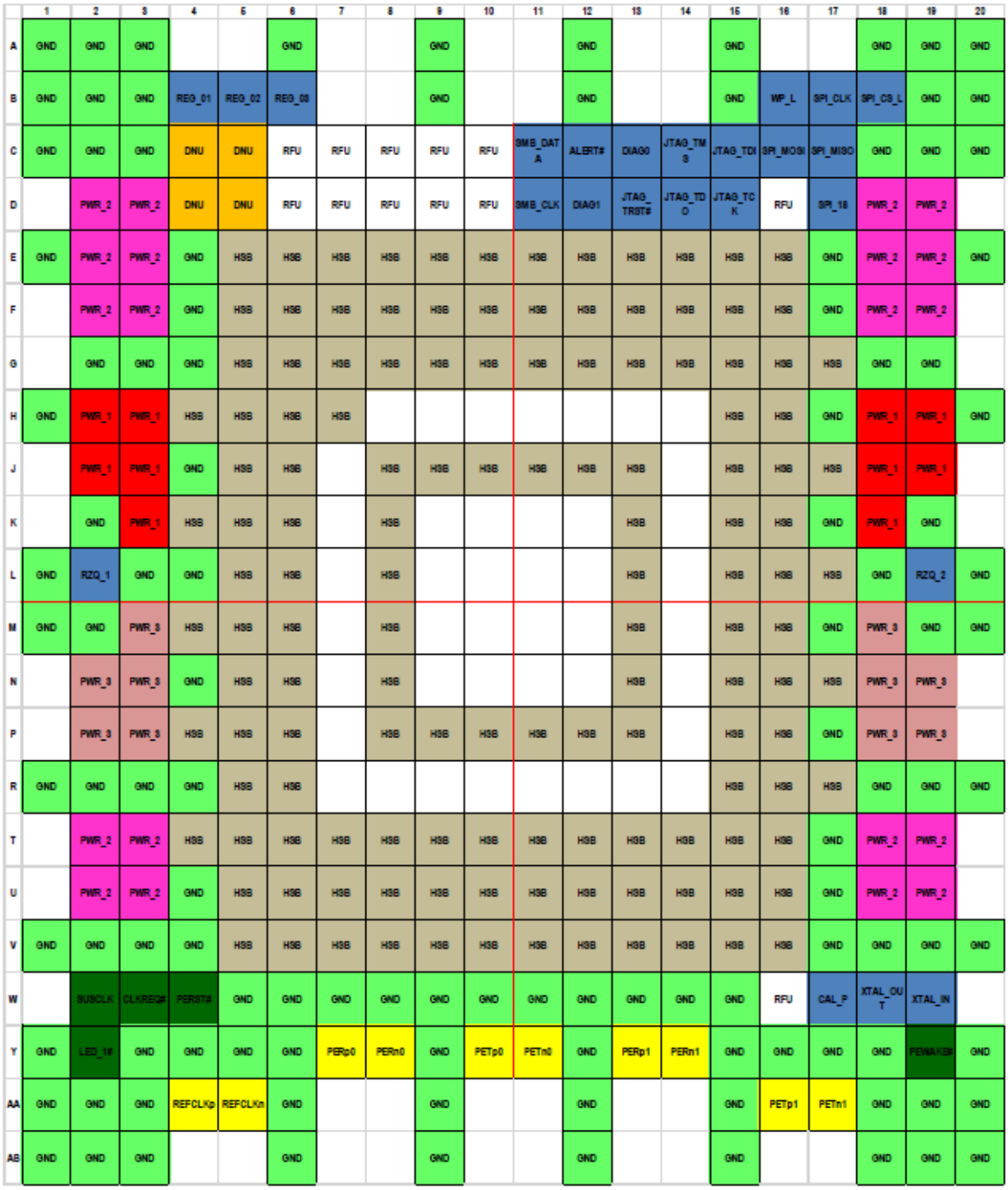


Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)

<Editor's Note: In Figure 105a replace text in cells:

C10: PLN#~~RFU~~

D10: PLA_S3#~~RFU~~>



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	GND
C	GND	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_1S	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PERp0	PERn0	GND	PETp0	PETn0	GND	PERp1	PERn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PETp1	PETn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND

Figure 105a. Type 1113 Module-side BGA Ballmap (Top View)

In Figure 111 replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- /PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B- /PERn0		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		~~1.2V~~ PWR_3	~~1.2V~~ PWR_3	GND	GND	~~1.2V~~ PWR_3	~~1.2V~~ PWR_3		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PERp2	PERn2		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		~~1.8V~~ PWR_2	~~1.8V~~ PWR_2	GND	GND	~~1.8V~~ PWR_2	~~1.8V~~ PWR_2		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1# / DAS	RFU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	~~3.3V~~ PWR_1	~~3.3V~~ PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

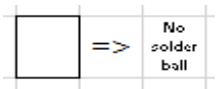


Figure 111. Type 1620 BGA Socket Map ~~Pinout~~ On Platform (Top View)

<Editor's Note: In Figure 112 replace text in cells:

H15: PLN#~~RFU~~

K15: PLA_S3#~~RFU~~>

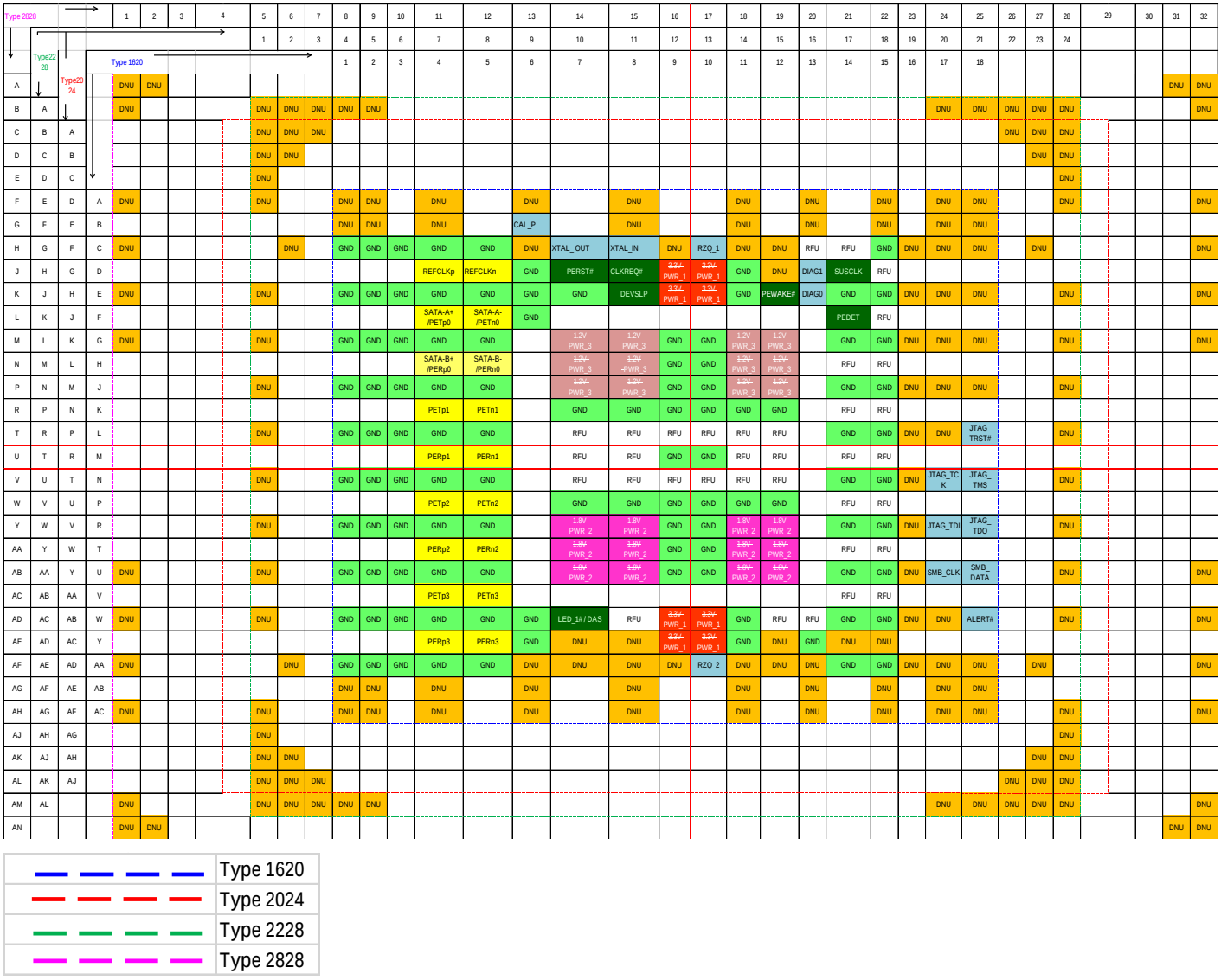


Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA ~~Pinout On Platform~~ Socket Map On Platform (Top View)

<Editor's Note: In Figure 1 replace text in cells:

C10: PLN#~~RFU~~

D10: PLA_S3#~~RFU~~>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	GND
C	GND	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PETp0	PETn0	GND	PERp0	PERn0	GND	PETp1	PETn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PERp1	PERn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND

Figure 1. Type 1113 BGA Socket Map On Platform (Top View)